RZ/A1H Group

Capture Engine Unit Sample Program

R01AN1824EJ0100
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Introduction

This application note describes the program which captures image data from an external camera module and transfers the data to memory by using the RZ/A1H's Capture Engine Unit (CEU).

Capture Engine Unit Sample Program offers the following features:

- Captures image data (a single frame) from the camera module.
- Uses the data enable fetch mode for capturing image data.
- Connects to the camera module via 16-bit I/F. (Note that the low-order 10 bits constitute effective data on the camera module.)
- Converts the 10-bit data into 8-bit data (by software processing which treats the high-order 8 bits as effective data).
- Always uses the A side of the CEU registers.
- Uses the Video Display Controller 5 (VDC5) to display 8-bit data as conversion results on the LCD.
- Displays a monochrome LCD image through the VDC5 CLUT.

Target Device

RZ/A1H

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

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1. Specifications

The sample code in this application note, One-frame of Image data is captured from an external camera module and is transferred to memory by using the RZ/A1H's Capture Engine Unit (CEU).The data is displayed on the LCD by VDC5. It is converted by the software and is displayed by VDC5 on the LCD. Table 1.1 shows Peripheral Functions and Their Applications.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Functions	Application
CEU	Captures image data.
INTC (interrupt ID: CEUI (364))	CEU interrupt
VDC5 (ch1) (layer 2)	Displays an image on the LCD.

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	RZ/A1H
Operating frequency*	CPU clock (Iϕ): 400MHz Image processing clock (Gϕ): 266.67MHz Internal bus clock (Bϕ): 133.33MHz Peripheral clock 1 (P1ϕ): 66.67MHz Peripheral clock 0 (P0ϕ): 33.33MHz
Operating voltage	Power supply voltage (I/O): 3.3V Power supply voltage (Internal): 1.18V
Integrated development environment	ARM® integrated development environment ARM Development Studio 5 (DS-5™) Version 5.16
C compiler	ARM C/C++ Compiler/Linker/Assembler Ver.5.03 [Build 102]
	Compiler options (excluding additional directory path) -O3 -Ospace --cpu=Cortex-A9 --littleend --arm --apcs=/interwork --no_unaligned_access --fpu=vfpv3_fp16 -g --asm
Operating mode	Boot mode 0 (CS0-space 16-bit booting)
Board used	GENMAI board ・RTK772100BC00000BR (R7S72100 CPU board) ・RTK7721000B00000BR (Option board for the R7S72100 CPU board)
Device used (functionality to be used on the board)	Camera module I/F (option board: J17) MT9V024 1/3-inch Wide-VGA Digital Image Sensor 752H x 480 V 10-bit column-parallel
	Display Out (Analog RGB D-sub 15) (Option board: J16)
	Serial interface (connected with a Dsub-9 connector)

Note: * The operating frequency used in clock mode 0 (Clock input of 13.33MHz from EXTAL pin)

3. Related Application Notes

For additional information associated with this document, refer to the following application note.

RZ/A1H Group Example of Initialization (R01AN1864EJ)

RZ/A1H Group Video Display Controller 5(VDC5) Sample Driver(R01AN1822EJ)

RZ/A1H Group I/O definition header file <iodefine.h> (R01AN1860EJ)

4. Peripheral Functions

The basic functions of the CEU and VDC4 are described in the RZ/A1H Group User's Manual: Hardware.

5. Hardware

5.1 Hardware Configuration

Figure 5.1 shows Examples of Hardware Devices Connected.

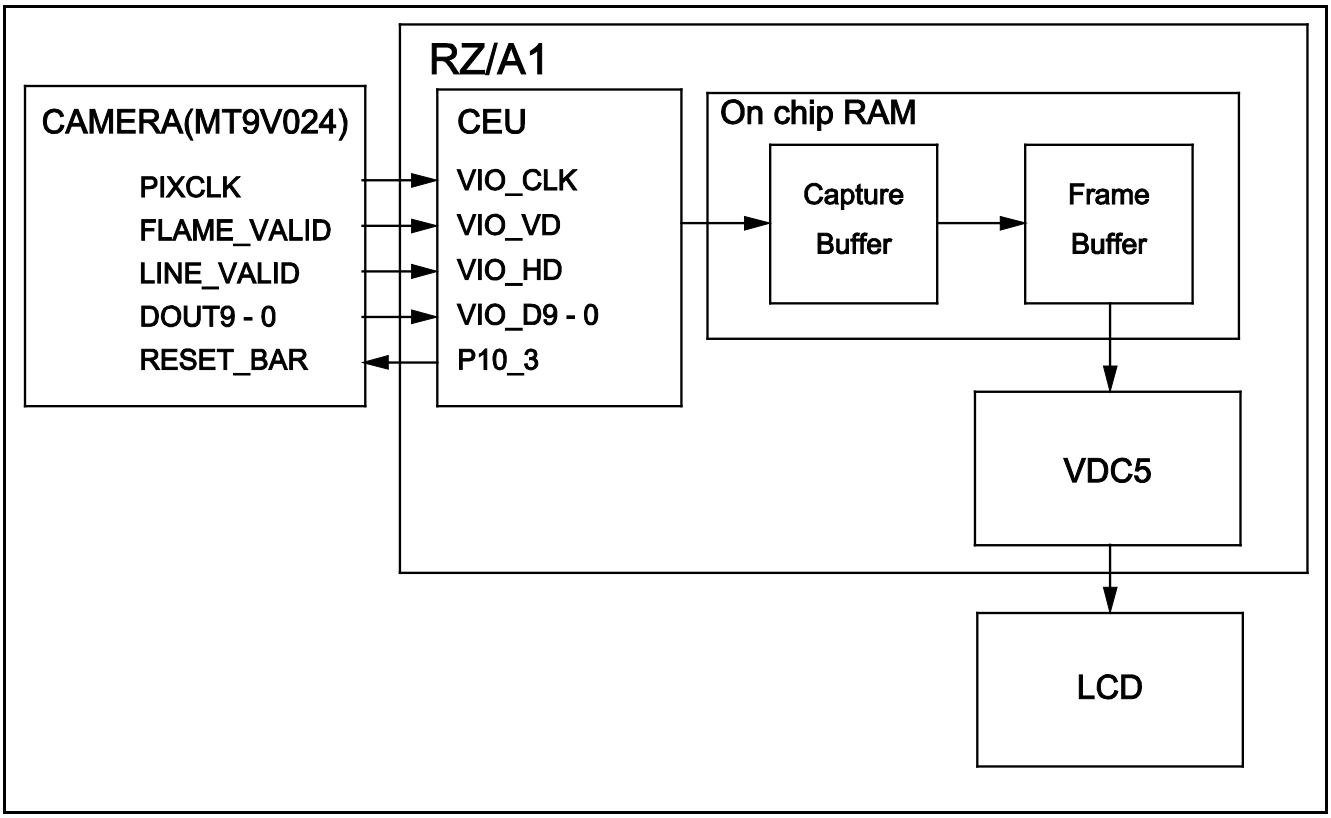

Figure 5.1 Examples of Hardware Devices Connected

5.2 Pins Used

Table 5.1 lists Pins Used and Their Functions.

Table 5.1 Pins Used and Their Functions

Pin Name	I/O	Function
P10_0	Input	VIO_CLK (6th alternative function) PIXCLK (on the camera)
P10_1	Input	VIO_VD (6th alternative function) FLAME_VALID (on the camera)
P10_2	Input	VIO_HD (6th alternative function) LINE_VALID (on the camera)
P10_3	Output	General-purpose output RESET_BAR (on the camera)
P10_4	Input	VIO_D0 (6th alternative function) DOUT0 (on the camera)
P10_5	Output	VIO_D1 (6th alternative function) DOUT1 (on the camera)
P10_6	Input	VIO_D2 (6th alternative function) DOUT2 (on the camera)
P10_7	Input	VIO_D3 (6th alternative function) DOUT3 (on the camera)
P10_8	Input	VIO_D4 (6th alternative function) DOUT4 (on the camera)
P10_9	Input	VIO_D5 (6th alternative function) DOUT5 (on the camera)
P10_10	Input	VIO_D6 (6th alternative function) DOUT6 (on the camera)
P10_11	Input	VIO_D7 (6th alternative function) DOUT7 (on the camera)
P10_12	Input	VIO_D8 (6th alternative function) DOUT8 (on the camera)
P10_13	Input	VIO_D9 (6th alternative function) DOUT9 (on the camera)
P10_14	NC	General-purpose output (low)
P10_15	NC	General-purpose output (low)
P11_0	NC	General-purpose output (low)
P11_1	NC	General-purpose output (low)
P11_2	NC	General-purpose output (low)
P11_3	NC	General-purpose output (low)

6. Software

6.1 Operational Overview

Using the CEU, this sample program transfers image data from the camera module to the on-chip RAM. After capturing one frame, it converts the data. On the VDC5, the conversion results become samples which can be displayed on the LCD.

The camera module (MT9V024) for this sample program is an image sensor which does not have R, G, and B values for each pixel. Image data from this camera module cannot therefore be displayed on the LCD without processing. Thus, by using brightness information for each pixel, the sample program processes image data to display 256-gradation monochrome data on the LCD.

6.1.1 Data capture timing

FRAME_VALID/LINE_VALID connected with VIO_VD/VIO_HD provides interface with the camera module (MT9V024). Data is captured in data enable fetch mode of the CEU. Data is captured through the CEU when VIO_HD is asserted (set to high) while VIO_VD is being high. Figure 6.1 and Table 6.1 show the timing when image data from the camera module (MT9V024) is output.

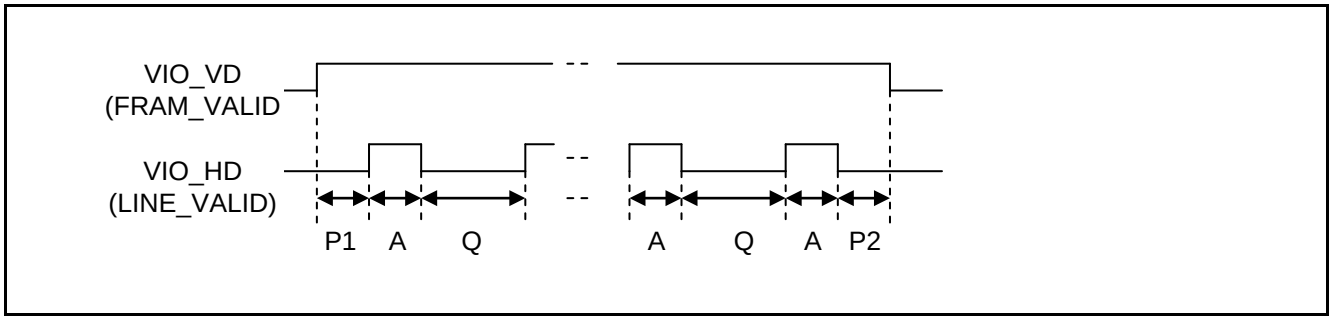

Figure 6.1 Row Timing and FRAME_VALID/LINE_VALID_Signal

Table 6.1 Frame Time

Parameter	Name	Default Timing
A	Active data time	752 pixel clocks
P1	Frame start blanking	72 pixel clocks
P2	Frame end blanking	23 pixel clocks
Q	Horizontal blanking	94 pixel clocks

6.1.2 Conversion of 10-bit data into 8-bit data

This sample program captures the low-order 10 bits of the 16-bit I/F as effective data from the camera module (MT9V024). It converts these 10 bits of data into 8-bit data to display 256-gradation monochrome data.

6.2 Memory Mapping

Figure 6.2 shows the Address Space of the RZ/A1H group and the Memory Mapping of the GENMAI board.

In this sample code, the code and data used in the ROM area is located in the NOR flash memory connected to the CS0 space, and the code and data used in the RAM area is located in the large-capacity on-chip RAM.

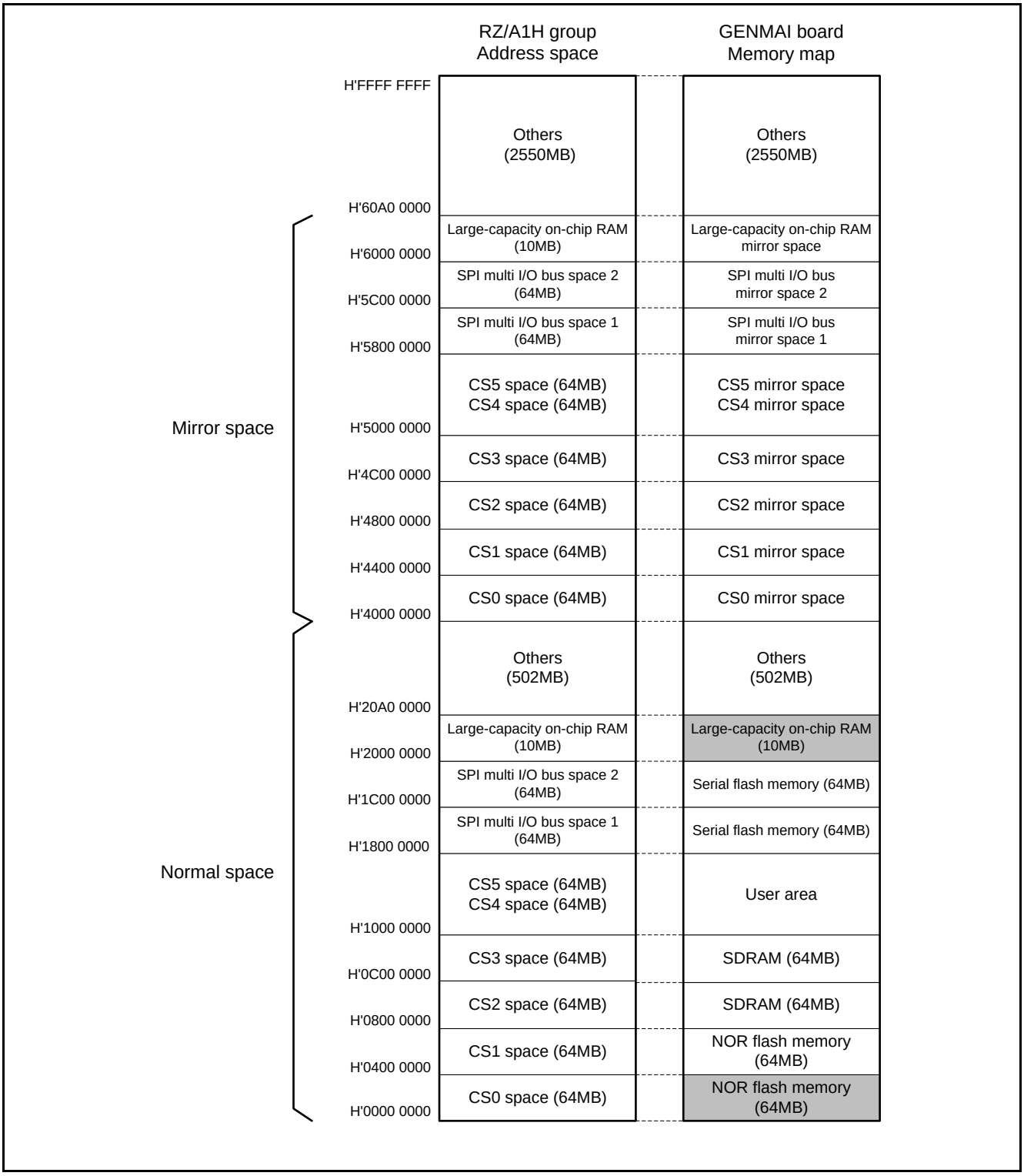

Figure 6.2 Memory Mapping

6.2.1 Section Assignment in Sample Code

In this sample code, the exception processing vector table and the IRQ interrupt handler are assigned to the large-capacity on-chip RAM, and they are executed in such RAM to speed up the interrupt processing. The transfer processing from the NOR flash memory area which is the program code of the exception processing vector table and the IRQ interrupt handler to the large-capacity on-chip RAM area, the clear to zero processing for the data selection without initial data, and the initialization for the data selection with initial data are executed by using the scatter-loading function. Refer to "Image structure and generation" in "ARM Compiler toolchain Using the Linker" provided by the ARM for more information about the scatter-loading function.

Table 6.2 and Table 6.3 list the Sections to be Used in this sample code. Figure 6.3 shows the Section Assignment for the initial condition of the sample code and the condition after using the scatter-loading function.

Table 6.2 Sections to be Used (1/2)

Area Name	Description	Type	Loading Area	Execution Area
VECTOR_TABLE	Exception processing vector table	Code	FLASH	FLASH
RESET_HANDLER	Program code area of reset handler processing This area consists of the following sections. • INITCA9CACHE (L1 cache setting) • INIT_TTB (MMU setting) • RESET_HANDLER (Reset handler)	Code	FLASH	FLASH
CODE_BASIC_SETUP	Program code area to optimize operating frequency and flash memory	Code	FLASH	FLASH
InRoot	This area consists of the sections located in the root area such as C standard library.	Code and RO Data	FLASH	FLASH
CODE_FPU_INIT	Program code area for NEON and VFP initializations This area consists of the following sections. • CODE_FPU_INIT • FPU_INIT	Code	FLASH	FLASH
CODE_RESET	Program code area for hardware initialization This area consists of the following sections. • CODE_RESET (Startup processing) • INIT_VBAR (Vector base setting)	Code	FLASH	FLASH
CODE_IO_REGRW	Program code area for read/write functions of I/O register	Code	FLASH	FLASH
CODE	Program code area for defaults All the Code type sections which do not define section names with C source are assigned in this area.	Code	FLASH	FLASH
CONST	Constant data area for defaults All the RO Data type sections which do not define section names with C source are assigned in this area.	RO Data	FLASH	FLASH

Table 6.3 Sections to be Used (2/2)

Area Name	Description	Type	Loading Area	Execution Area
VECTOR_MIRROR_TABLE	Exception processing vector table (Section to transfer data to large-capacity on-chip RAM)	Code	FLASH	LRAM
CODE_HANDLER_JMPTBL	Program code area for user-defined functions of IRQ interrupt handler	Code	FLASH	LRAM
CODE_HANDLER	Program code area of IRQ interrupt handler This area consists of the following sections. • CODE_HANDLER • IRQ_FIQ_HANDLER	Code	FLASH	LRAM
DATA_HANDLER_JMPTBL	Registration table data area for user-defined functions of IRQ interrupt handler	RW Data	FLASH	LRAM
ARM_LIB_STACK	Application stack area	ZI Data	-	LRAM
IRQ_STACK	IRQ mode stack area	ZI Data	-	LRAM
FIQ_STACK	FIQ mode stack area	ZI Data	-	LRAM
SVC_STACK	Supervisor (SVC) mode stack area	ZI Data	-	LRAM
ABT_STACK	Abort (ABT) mode stack area	ZI Data	-	LRAM
TTB	MMU translation table area	ZI Data	-	LRAM
ARM_LIB_HEAP	Application heap area	ZI Data	-	LRAM
DATA	Data area with initial value for defaults All the RW Data type sections which do not define section names with C source are assigned in this area.	RW Data	FLASH	LRAM
BSS	Data area without initial value for defaults All the ZI Data type sections which do not define section names with C source area assigned in this area.	ZI Data	-	LRAM
VRAM	Display Buffer	Data	-	LRAM
CEU_BUFFER	Capture Buffer	Data	-	LRAM

Notes: 1. "FLASH" and "LRAM" shown in Loading Area and Execution Area indicate the NOR flash memory area and the large-capacity on-chip RAM area respectively.

2. Basically the section name is set to be the same as the region's, however it consists of some sections in the areas of RESET_HANDLER, InRoot, CODE_FPU_INIT, CODE_RESET, CODE, CONST, CODE_HANDLER, DATA, and BSS. Refer to the ARM compiler toolchain manual about the region and the section.

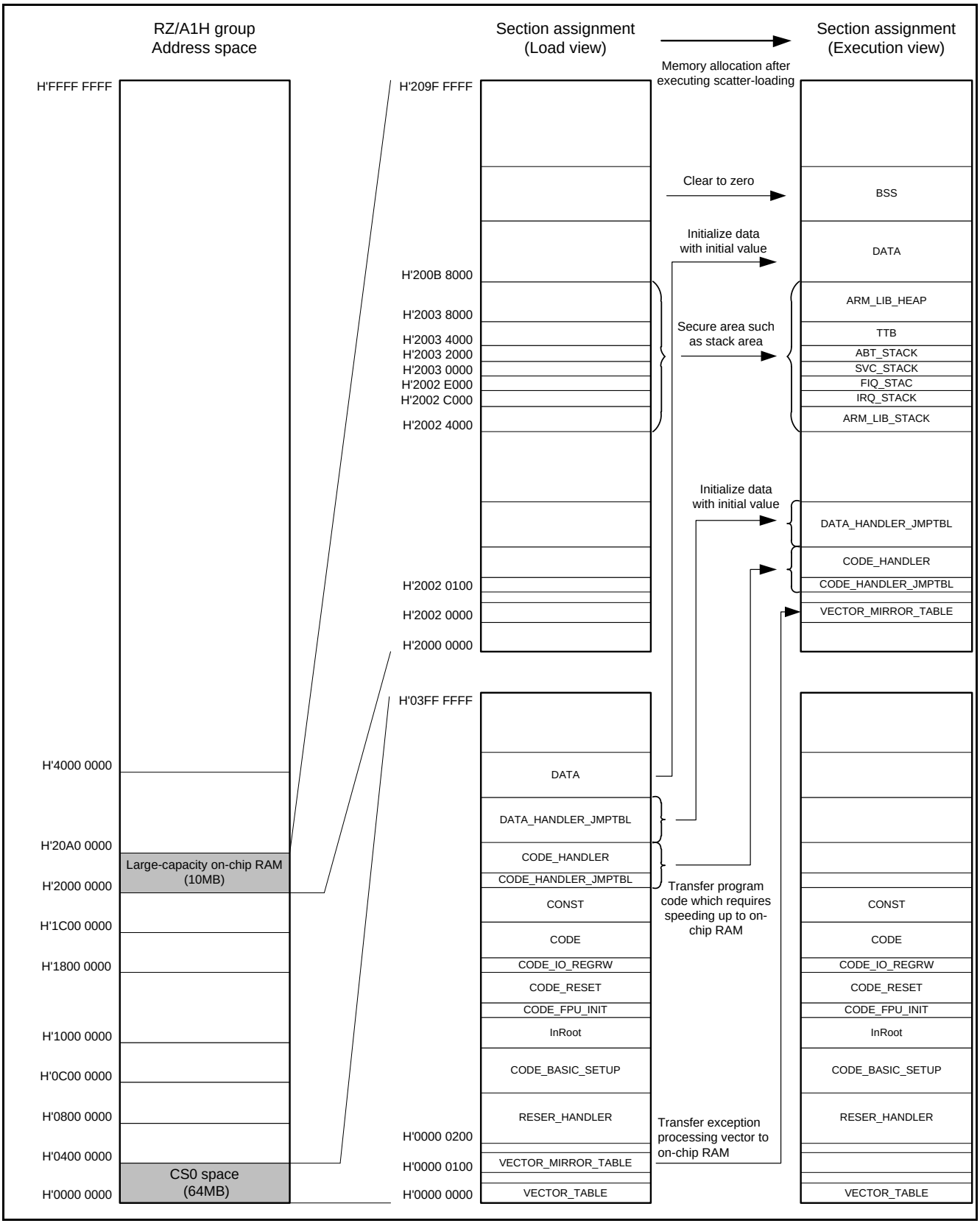

Figure 6.3 Section Assignment

6.2.2 Setting for MMU

The MMU is set to manage the 4 GB area in 1MB unit from the address H'0000 0000 in response to the memory map of the hardware resource used for the GENMAI board. (Set by the ttb_init.s file.) The minimum unit should be 1MB when customizing the MMU based on the system.

Table 6.4 lists the Setting for MMU.

Table 6.4 Setting for MMU

Definition Name	Contents	Address	Size	Memory Type
M_SIZE_NOR	CS0 and CS1 spaces (NOR flash memory)	H'0000 0000 to H'07FF FFFF	128MB	L1 cache enable, Normal memory
M_SIZE_SDRAM	CS2 and CS3 spaces (SDRAM)	H'0800 0000 to H'0FFF FFFF	128MB	L1 cache enable, Normal memory
M_SIZE_CS45	CS4 and CS5 spaces	H'1000 0000 to H'17FF FFFF	128MB	Strongly-ordered memory (L1 cache disable)
M_SIZE_SPI	SPI multi IO bus space 1 and 2 (serial flash memory)	H'1800 0000 to H'1FFF FFFF	128MB	L1 cache enable, Normal memory
M_SIZE_RAM	Large-capacity on-chip RAM space	H'2000 0000 to H'209F FFFF	10MB	L1 cache enable, Normal memory
M_SIZE_IO_1	On-chip peripheral module and reserved area	H'20A0 0000 to H'3FFF FFFF	502MB	Strongly-ordered memory (L1 cache disable)
M_SIZE_NOR_M	CS0 and CS1 mirror spaces	H'4000 0000 to H'47FF FFFF	128MB	L1 cache disable, Normal memory
M_SIZE_SDRAM_M	CS2 and CS3 mirror spaces	H'4800 0000 to H'4FFF FFFF	128MB	L1 cache disable, Normal memory
M_SIZE_CS45_M	CS4 and CS5 mirror spaces	H'5000 0000 to H'57FF FFFF	128MB	Strongly-ordered memory (L1 cache disable)
M_SIZE_SPI_M	SPI multi IO bus mirror space 1 and 2	H'5800 0000 to H'5FFF FFFF	128MB	L1 cache disable, Normal memory
M_SIZE_RAM_M	Large-capacity on-chip RAM mirror space	H'6000 0000 to H'609F FFFF	10MB	L1 cache disable, Normal memory
M_SIZE_IO_2	On-chip peripheral module and reserved area	H'60A0 0000 to H'FFFF FFFF	2550MB	Strongly-ordered memory (L1 cache disable)

6.3 Interrupts

Table 6.5 shows interrupts for the sample code.

Table 6.5 Interrupts for the Sample Code

Interrupt (source ID)	Priority	Process outline
INTC_ID_CEUI	5	1-frame capture end report

6.4 Fixed-Width Integers

Table 6.6 shows the Fixed-Width Integers Used in Sample Code.

Table 6.6 Fixed-Width Integers Used in Sample Code

Symbol	Contents
char_t	8-bit character
bool_t	Boolean type, value: true (1) or false (0)
int_t	High-speed integer, signed 32-bit integer in this sample code
int8_t	8-bit integer, singed (Defined by standard library)
int16_t	16-bit integer, singed (Defined by standard library)
int32_t	32-bit integer, singed (Defined by standard library)
int64_t	64-bit integer, singed (Defined by standard library)
uint8_t	8-bit integer, unsigned (Defined by standard library)
uint16_t	16-bit integer, unsigned (Defined by standard library)
uint32_t	32-bit integer, unsigned (Defined by standard library)
uint64_t	64-bit integer, unsigned (Defined by standard library)
float32_t	32-bit floating point (Defined by standard library when specifying "__ARM_NEON__")
float64_t	64-biy floating point (Defined by standard library) (Defined by standard library when specifying "__ARM_NEON__")
float128_t	128-bit floating point

6.5 List of Constants and Error Codes

Table 6.7 lists the constants for the sample program. Table 6.8 lists the error codes for the sample code.

Table 6.7 Constants for the Sample Program

Constant	Setting	Description
CEU_CONFIG_ CAPTURE_SCREEN_ HSYNC_NUM_PXL	752u	Horizontal effective data area for Camera module. In this sample, don't change value.
CEU_CONFIG_ CAPTURE_SCREEN_ VSYNC_NUM_PXL	480u	Vertical effective data area for Camera module. In this sample, don't change value.
CEU_INTERRUPT_ PRIORITY	5u	CEU interrupt priority
CAPTURE_END	1u	1-frame capture end flag.
CEU_CAPTUER_ BUFF_STRIDE	(((CEU_CONFIG_CAPTURE_SCREEN_HSYNC_NUM_PXL) + 31u) & ~0x001Fu)	CEU capture buffer stride. 32 byte unit
CEU_CAPTUER_ BUFF_HEIGHT	CEU_CONFIG_CAPTURE_SCREEN_VSYNC_NUM_PXL	Height of capture buffer.
CEU_BURST_MODE_X1	0u	Data transfer unit to the bus bridge Transfer to bus 32 bytes
CEU_SIGNAL_ HIGH_ACTIVE	0u	Polarity of the sync signal (positive polarity)
CEU_SIGNAL_ LOW_ACTIVE	1u	Polarity of the sync signal (negative polarity)
CEU_DATAOUT_ SWAP_DISABLE	0u	Data is not swapped.
CEU_DATAOUT_ SWAP_ENABLE	1u	Data is swapped.
CEU_INT_ ONE_FRAME_ CAPTUER_END	0x00000001uL	One-Frame Capture End Interrupt Enable
CEU_CONFIG_ BURST_MODE	CEU_BURST_ MODE_X1	Capture Control Register (CAPCR.MTCM[1:0]) Transferred to the bus in 32-byte units
CEU_CONFIG_ 32BIT_DATA_SWAP	CEU_DATAOUT_ SWAP_ENABLE	Capture Data Output Control Register (CDOCR.COLS) Swap of 32-bit units
CEU_CONFIG_ 16BIT_DATA_SWAP	CEU_DATAOUT_ SWAP_ENABLE	Capture Data Output Control Register (CDOCR.COWS) Swap of 16-bit units
CEU_CONFIG_ 8BIT_DATA_SWAP	CEU_DATAOUT_ SWAP_DISABLE	Capture Data Output Control Register (CDOCR.COBS) Swap of 8-bit units
CEU_CONFIG_ CAMERA_SIGNAL_ POLARITY_VD	CEU_SIGNAL_ HIGH_ACTIVE	Capture Interface Control Register (CAMCR.VDPOL) Polarity of the sync signal (positive polarity)
CEU_CONFIG_ CAMERA_SIGNAL_ POLARITY_HD	CEU_SIGNAL_ HIGH_ACTIVE	Capture Interface Control Register (CAMCR.HDPOL) Polarity of the sync signal (positive polarity)

Constant	Setting	Description
CEU_CONFIG_ CAPTURE_MODE	CEU_SINGLE_ CAPTURE	Capture Control Register (CAPCR.CTNCP) 1-frame capture mode

Table 6.8 Error Codes for the Sample Code

Constant	Setting	Description
CEU_ERROR_OK	0	Success
CEU_ERROR_PARAM	-1	Parameter error

6.6 List of Variables

Table 6.9 lists the static variables.

Table 6.9 static Variables

Type	Variable Name	Contents	Function Used
uint16_t	CaptureBuffer	CEU capture buffer for captured image data	CEU_SAMPLE_ CeuConvertbitRgbData()
uint8_t	FrameBuffer	VDC5 LCD display buffer for output from the VDC5	CEU_SAMPLE_ CeuConvertbitRgbData()
uint32_t	g_ceu_complete_flag	1-frame capture end report	CEU_SAMPLE_ CeuSingleCapture()
uint32_t	g_ceu_error_flag	Unused-interrupt report	CEU_SAMPLE_ CeuSingleCapture()

6.7 List of Functions

Table 6.10 shows List of Functions.

Table 6.10 List of Functions

Function name	Page number
R_CEU_ModuleInit	18
R_CEU_ConfigInit	18
R_CEU_SetMemoryAddress	18
R_CEU_CallbackISR	19
R_CEU_CaptureStart	19
R_CEU_InterruptEnable	19
R_CEU_InterruptDisable	19
CEU_SAMPLE_CeuSingleCaptureInit	20
CEU_SAMPLE_CeuSingleCapture	20
CEU_SAMPLE_CeuConvert8bitRgbData	21

6.8 Function Specifications

This section contains the specifications for the functions that are implemented in the sample code.

6.8.1 R_CEU_ModuleInit

R_CEU_ModuleInit		
Synopsis	CEU module pre-initialization.	
Header	r_ceu.h	
Declaration	void R_CEU_ModuleInit(void (*init_func)(void))	
Description	In this function, the operations are performed as below. - The specified user-defined function is executed. - Clock supply to CEU is enabled.	
Arguments	init_func	: Pointer to the user-defined function
Return value	None	

6.8.2 R_CEU_ConfigInit

R_CEU_ConfigInit	
Synopsis	CEU module initialization.
Header	r_ceu.h
Declaration	void R_CEU_ConfigInit(void)
Description	In this function, the operations are performed as below. - CEU setting for the camera module as below. [Camera (APTINA MT9V024) Spec] - VD/HD signal polarity = Active high - Bus width = 10 bits - Pixel output timing = Data fetch mode (Blank period = 0 HD) - Active pixels = 752 H x 480 V
Arguments	None
Return value	None

6.8.3 R_CEU_SetMemoryAddress

R_CEU_SetMemoryAddress		
Synopsis	The function which sets the address of capture data buffer.	
Header	r_ceu.h	
Declaration	ceu_error_t R_CEU_SetMemoryAddress(uint32_t addr)	
Description	In this function, the operations are performed as below. -The address of a capture data buffer is set. The buffers must be 4 byte boundaries.	
Arguments	addr	: The address of a capture data buffer.
Return value	Error code	

6.8.4 R_CEU_CallbackISR

R_CEU_CallbackISR		
Synopsis	CEU driver set interrupt callback function.	
Header	r_ceu.h	
Declaration	void R_CEU_CallbackISR(void (*callback)(uint32_t))	
Description	In this function, the operations are performed as below. -Setting interrupt callback function.	
Arguments	callback	: Pointer to the user-defined function.
Return value	None	

6.8.5 R_CEU_CaptureStart

R_CEU_CaptureStart	
Synopsis	The function which start capture.
Header	r_ceu.h
Declaration	void R_CEU_CaptureStart(void)
Description	In this function, the operations are performed as below. -This function starts CEU capture.
Arguments	None
Return value	None

6.8.6 R_CEU_InterruptEnable

R_CEU_InterruptEnable		
Synopsis	The function which enables interrupt for data enable capture mode.	
Header	r_ceu.h	
Declaration	void R_CEU_InterruptEnable(uint32_t flag)	
Description	In this function, the operations are performed as below. -This function enables CEU interrupt.	
Arguments	Flag	: CEIER reg set value.
Return value	None	

6.8.7 R_CEU_InterruptDisable

R_CEU_InterruptDisable	
Synopsis	The function which disables interrupt for data enable capture mode.
Header	r_ceu.h
Declaration	void R_CEU_InterruptDisable(void)
Description	In this function, the operations are performed as below. -This function disables CEU interrupt.
Arguments	None
Return value	None

6.8.8 CEU_SAMPLE_CeuSingleCaptureInit

Graphics_CeuSingleCaptureInit	
Synopsis	CEU module initialization.
Header	ceu_sample.h
Declaration	void Graphics_CeuSingleCaptureInit(void)
Description	In this function, the operations are performed as below. - R_CEU_ModuleInit Function call. - R_CEU_ConfigInit Function call. - R_CEU_CallbackISR Function call. - R_CEU_InterruptEnable Function call. - Registration of the interrupt function.
Arguments	None
Return value	None

6.8.9 CEU_SAMPLE_CeuSingleCapture

Graphics_CeuSingleCapture	
Synopsis	CEU Single Capture Start.
Header	ceu_sample.h
Declaration	void Graphics_CeuSingleCapture(uint16_t *pCapBuff)
Description	In this function, the operations are performed as below. - R_CEU_SetMemoryAddress Function call. - R_CEU_CaptureStart Function call. - Wait for end of capture.
Arguments	pCapBuff : Pointer of capture buffer.
Return value	None

6.8.10 CEU_SAMPLE_CeuConvert8bitRgbData

Graphics_CeuConvert8bitRgbData

Synopsis	Conversion of 16-bit data to 8-bit data
Header	ceu_sample.h
Declaration	void Graphics_CeuConvert8bitRgbData (uint16_t *pSrcBuff, uint8_t *pDstBuff, uint16_t stride)
Description	This function is converted to 8-bit data from 16-bit data. CEU is 16-bit mode. Camera (APTINA MT9V024) is 10bit bus width. Capture data is as follows. [16bit Data] |----- 1 pixel ----| |----- 1 pixel ----| |----- 1 pixel ----| 0000 00XX XXXX XXxx, 0000 00XX XXXX XXxx, 0000 00XX XXXX XXxx, higher 8 bits (bit[10:2]) are effective. [8bit Data] | -- 1pixel -- | |-- 1pixel -- | |-- 1pixel -- | XXXX XXXX, XXXX XXXX, XXXX XXXX
Arguments	pSrcBuff : capture data (16-bit bus width) pDstBuff : VRAM buffer (8-bit data after conversion.) stride : pDstBuff stride.
Return value	None

6.9 Flowcharts

6.9.1 Main Processing

Figure 6.4 shows the main processing described in this application note.

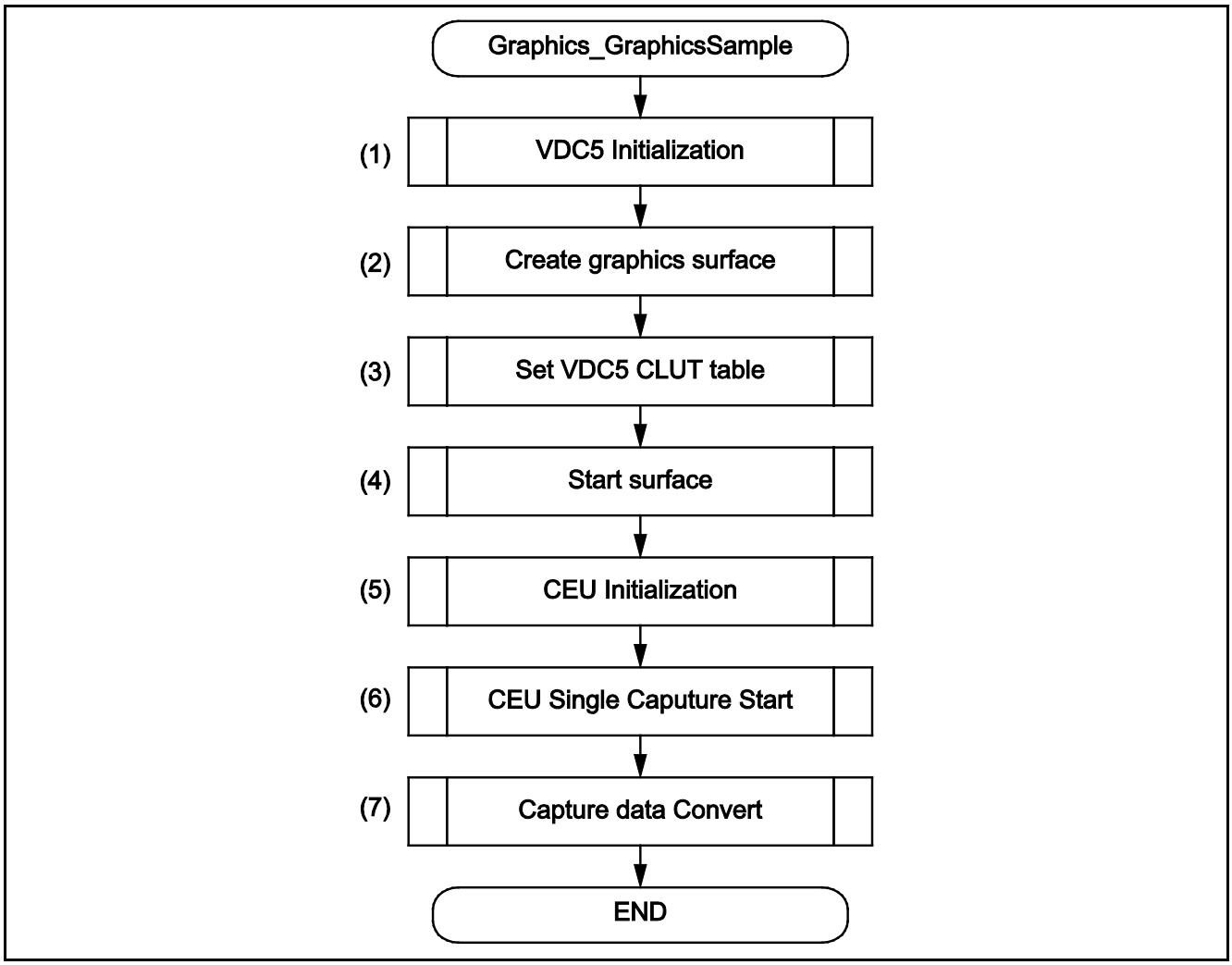

Figure 6.4 Main Processing

(1)～(4)：VDC5 initialization and Display Setting.

(5) ：CEU initialization.

(6) ：Capturing one frame image data output from the camera.

(7) ：Converts the data captured. Transfers it to the display buffer memory.

7. Sample Code

The sample code is available on the Renesas Electronics Website.

8. Documents for Reference

User's Manual: Hardware

RZ/A1H Group User's Manual: Hardware
The latest version can be downloaded from the Renesas Electronics website.

R7S72100 RTK772100BC00000BR (GENMAI) User's Manual
The latest version can be downloaded from the Renesas Electronics website.

R7S72100 CPU (GENMAI) Optional Board RTK7721000B00000BR User's Manual
The latest version can be downloaded from the Renesas Electronics website.

ARM Architecture Reference Manual ARMv7-A and ARMv7-R edition Issue C
The latest version can be downloaded from the ARM website.

ARM Generic Interrupt Controller Architecture Specification Architecture version 1.0
The latest version can be downloaded from the ARM website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

User's Manual: Development Tools

ARM Software Development Tools (ARM Compiler toolchain, ARM DS-5 etc) can be downloaded from the ARM website.
The latest version can be downloaded from the Renesas Electronics website.

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REVISISON HISTORY	RZ/A1H Group Capture Engine Unit Sample Program

Rev.	Date	Description	
		Page	Summary
1.00	May 28,2014	—	First edition issued

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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